

## CLAIMS

What is claimed is:

- 1 1. A substrate imprint tool, comprising:  
2 a light transparent base; and  
3 a light blocking distal end coupled to the light transparent base.
- 1 2. The substrate imprint tool of claim 1, further comprises a light transparent neck  
2 component formed between the light blocking distal end and the light transparent base.
- 1 3. The substrate imprint tool of claim 2, wherein the light transparent neck  
2 component to define a trace recess.
- 1 4. The substrate imprint tool of claim 2, wherein the light transparent neck  
2 component comprises of glass.
- 1 5. The substrate imprint tool of claim 2, wherein the light transparent neck  
2 component is wider than the light blocking distal end.
- 1 6. The substrate imprint tool of claim 1, wherein the light transparent base  
2 comprises of glass.
- 1 7. The substrate imprint tool of claim 1, wherein the light blocking distal end is to  
2 define a via recess.
- 1 8. The substrate imprint tool of claim 1, wherein the light blocking distal end further  
2 comprises a light transparent core coated with a light blocking material.
- 1 9. The substrate imprint tool of claim 1, wherein the light blocking distal end  
2 comprises a light transparent core with a bottom surface coated with a light blocking  
3 material.

- 1 10. The substrate imprint tool of claim 1, wherein the light blocking distal end  
2 comprises of a metal.
- 1 11. The substrate imprint tool of claim 9, wherein the metal is a selected one of  
2 chrome, aluminum, titanium, copper, gold and nickel.
- 1 12. A method, comprising:  
2 forming a dielectric layer on a core; and  
3 simultaneously imprinting and at least partially curing a circuitry feature onto the  
4 dielectric layer.
- 1 13. The method of claim 12, further comprises removing uncured dielectric material  
2 from the circuitry feature.
- 1 14. The method of claim 13, wherein the uncured dielectric material is a chad.
- 1 15. The method of claim 13, wherein the removing of uncured dielectric material from  
2 the circuitry feature further comprises dissolving the uncured dielectric material with a  
3 solvent that dissolves uncured dielectric material but does not dissolve cured dielectric  
4 material.
- 1 16. The method of claim 12, wherein the simultaneous imprinting and at least partial  
2 curing of circuitry feature further comprises imprinting a via recess.
- 1 17. The method of claim 12, wherein the simultaneous imprinting and at least partial  
2 curing of circuitry feature further comprises imprinting a trace recess.
- 1 18. The method of claim 17, wherein the simultaneous imprinting and at least partial  
2 curing of circuitry feature further comprises curing walls of the trace recess.

1 19. The method of claim 12, wherein the simultaneous imprinting and at least partial  
2 curing of circuitry feature further comprises partial UV curing.

1 20. A package substrate, comprising:  
2 a rigid core;  
3 a dielectric layer formed on the rigid core; and  
4 a circuitry feature formed in the dielectric layer by simultaneously imprinting and  
5 partially curing of the dielectric layer.

1 21. The package substrate of claim 20, wherein the circuitry feature formed in the  
2 dielectric layer by simultaneously imprinting and partially curing of the dielectric layer is  
3 formed further by using a substrate imprint tool comprising a light transparent base and  
4 a light blocking distal end coupled to the light transparent base.

1 22. The package substrate of claim 20, wherein the circuit component formed  
2 comprises a via recess.

1 23. The package substrate of claim 22, wherein the circuit component formed further  
2 comprises a trace recess coupled to the via recess.

1 24. The package substrate of claim 20, wherein the dielectric material is a  
2 crosslinkable polymer dielectric.

1 25. The package substrate of claim 20, wherein the circuitry feature formed in the  
2 dielectric layer by simultaneously imprinting and partially curing of the dielectric layer is  
3 further formed by UV partial curing.

1 26. A system, comprising:  
2 a package substrate, including  
3 a rigid core;  
4 a dielectric layer formed on the rigid core; and

5           a circuitry feature formed in the dielectric layer by simultaneously imprinting  
6           and partially curing of the dielectric layer;  
7       a bus coupled to the package substrate; and  
8       a networking interface coupled to the bus.

1   27.   The system of claim 26, wherein the circuitry feature formed comprises a via  
2   recess.

1   28.   The system of claim 27, wherein the circuitry feature further comprises a trace  
2   recess coupled to the via recess.

1   29.   The system of claim 26, wherein the dielectric material is a crosslinkable polymer  
2   dielectric.